Data Sheet

IRIS:

Fast EM Simulation with Virtuoso Integration

In high frequency silicon circuit design, passive devices, interconnect, and their mutual coupling have to be taken into account via electromagnetic (EM) simulation. Full-wave EM simulation is becoming necessary to cover the RF frequency of interest including multiple harmonics compared to quasi-static RC extraction. Cadence Virtuoso based schematic and layout flow is widely adopted for IC designers. However, lack of the built-in full-wave EM simulation tool leads to frequent transfer of the layout data between Virtuoso environment and outside EM tools, which is very manual and error-prone. The fast 3D method of moments solver with both multi-core and distributed parallelization greatly reduces the EM simulation time thus improves the design efficiency. The seamless integration with Virtuoso not only enables designers to stay in the Cadence design environment to perform the EM simulation which avoids the manual and error-prone layout data conversion, but also realizes the perfect convergence to front-end for design verification by automatic back-annotation. This design flow will greatly help IC designers to reduce the design cycles and achieve first-pass silicon success.

IRIS Solution

Xpeedic IRIS provides high frequency silicon design engineer a 3D fast EM simulation tool integrated in Cadence Virtuoso design flow to analyze on-chip passive devices. IC designers now have an automated way to access EM analysis of passive devices without limiting them to any specific PDK. IRIS is now an indispensable tool for the modern designer.

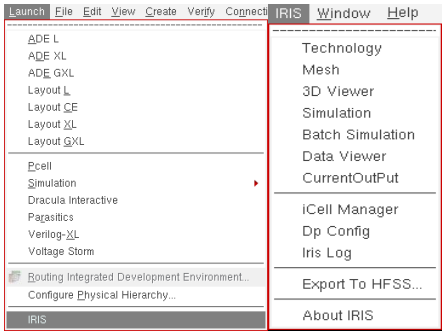
Key Points

- Accelerated 3D planar EM solver based on the Method of Moment (MoM) delivers the best performance in both speed and accuracy. It captures all the conductor and dielectric effects which are crucial for advanced nodes such as 45nm and below
- Seamless integration with Cadence Virtuoso enables designers to stay in the Cadence design environment to perform the EM simulation.
- Support bias table and rho table in IRIS to account for technology variations for advanced IC nodes.
- Automatically port searching and definition simplifies EM simulation setup.
- Support horizontal current switch to improve simulation efficiency for 3D mode.
- Support set metal model and shielding option layer by layer based on metal thickness, width and spacing.
- Support multi-threading technology when build Green's function to greatly improve the database creation efficiency and speed.
- Optimized mesh to balance speed and accuracy, support rectangle and triangle mixed mesh to improve simulation speed and convergence.
- Automatically disfeaturing via array when generate mesh file makes the geometry more EM-friendly.
- Support 3D model and current density display enable users to review the current distribution of device, which provides physical insights.
- Support parallel processing techniques, including multi-threading processing and distributed processing to improve solver performance speedup and efficiency, and fully utilize hardware computing resources.
- Support batch simulation when multiple simulation jobs exist.
- Support EM simulation results back-annotation.
- Easy export IRIS simulation project to HFSS and HFSS 3D Layout with tuned simulation setting to ensure accuracy.
- SnpExpert provides powerful S-Parameter post-process capability.

FEATURES

IRIS Menu

IRIS design flow is seamless integration with Cadence Virtuoso design environment. After start Virtuoso and click IRIS in “Launch” menu under layout editing window, an “IRIS” menu and iCell Manager Window will show up.



IRIS Menu

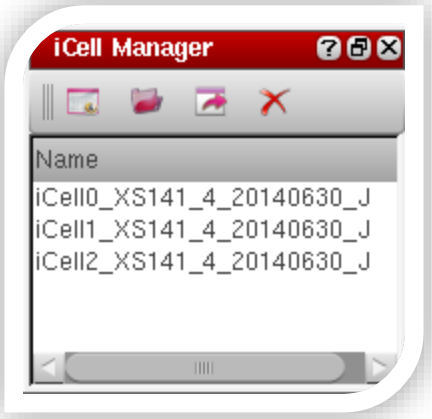
IRIS Virtuoso Interface

User can configure all mesh and simulation parameters through IRIS Virtuoso Interface after start IRIS successfully. IRIS simulation setting windows is quite easy, most of them are set automatically based on physical parameters.

IRIS Virtuoso Interface

iCell Manager

In IRIS, after open layout view of any cell, user should select part of the design for EM simulation, IRIS will convert it to iCell automatically under iCell Manager window’s management.

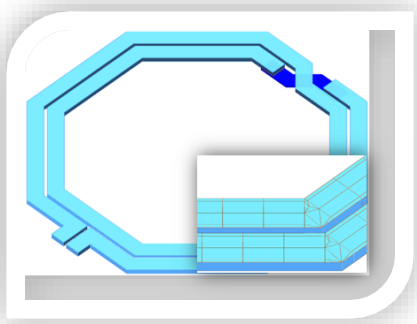


iCell Manager

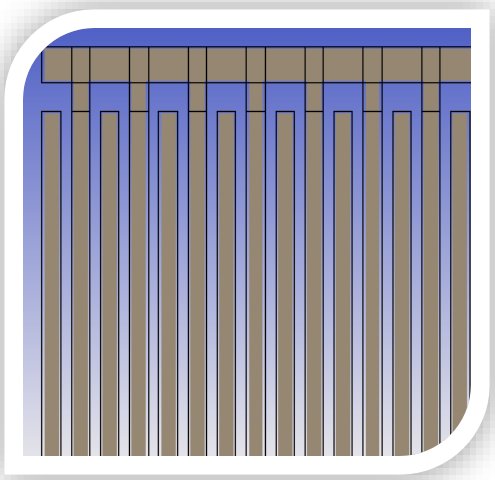
Optimal Mesh Technology

iCell generated from Virtuoso layout for EM simulation use optimized mesh to balance speed and accuracy, IRIS mesher support rectangle and triangle mixed

mesh to improve simulation speed and convergence. IRIS 3dview support 3D view of both layout structure and mesh.



Mesh View



Biased Mesh

3D EM Solver

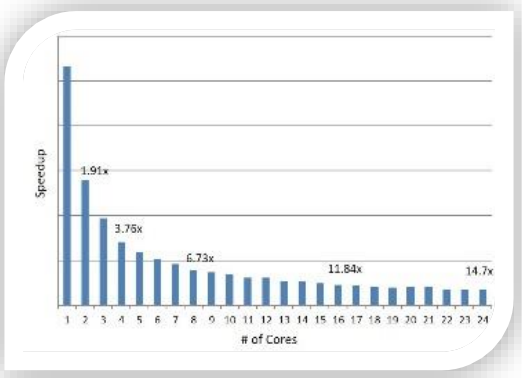
IRIS deploys a fast 3D full-wave Method-of-Moment (MoM) based EM solvers which delivers both speed and accuracy, and support 3D mode simulation to capture sidewall effect, and make it suitable for 45nm technology and below.

Advanced Technology Variation

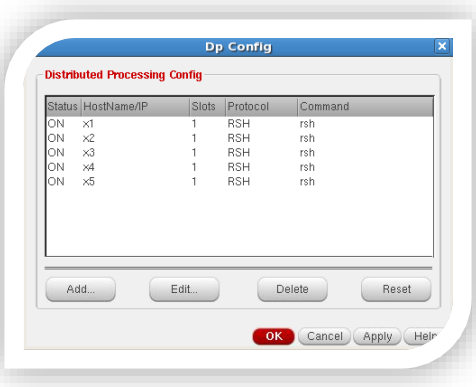
In advanced process technology, metal conductivity and width was not fixed since technology variation. IRIS support both rho table and bias table defined in process file to account for conductivity and geometry variation effect.

Parallel Processing Technique

In addition to the fast computation technology used in solver, IRIS also supports parallel processing technology to reduce simulation time. Both of distributed processing and multi-core processing are available, which can further increase the simulation efficiency with the update of computer hardware environment.



Multicore Speedup



Parallel Processing Option

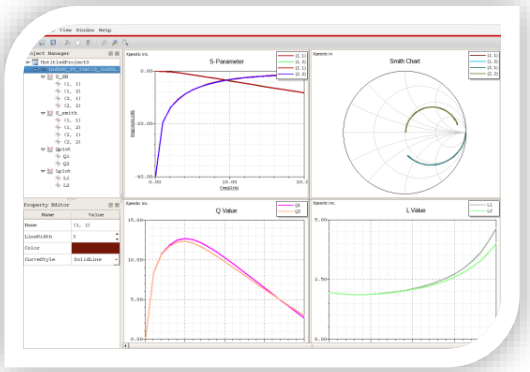
Export to Ansys Project

Provides one-click solution to export IRIS simulation project to HFSS and HFSS 3D Layout with tuned simulation settings to ensure accuracy as part of Xpeedic and Ansys software partnership. A unified IRIS2HFSS and IRIS2HFSS3DLayout window will popup for user to do some basic EM setups, including extents, ground ring, air box, solver inside and so on. The converted HFSS and HFSS 3D Layout project is ready to run with no need of manual editing.

Export to Ansys

Post Process

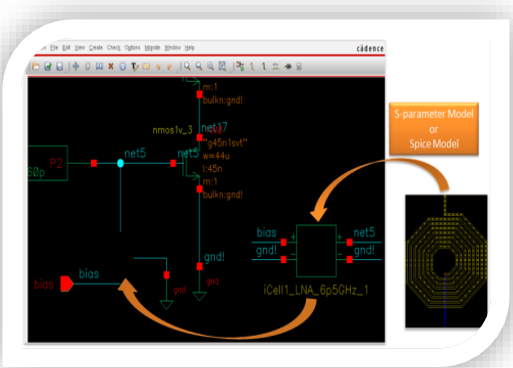
SnpExpert provides powerful S-parameter post-process capability. The template function enables user to plot by one click. Equivalent circuit model and broadband SPICE model can be exported in addition to S-parameter.



Waveform Display

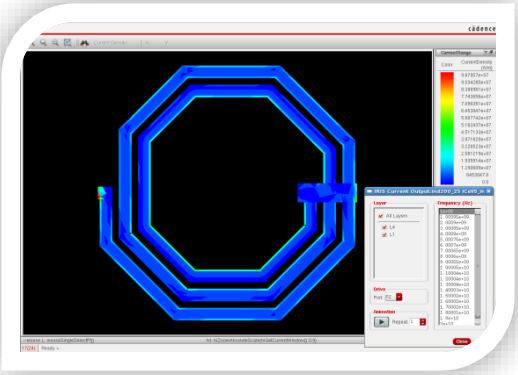
Back Annotation

Back annotation performs to modify part of the original circuit with S-parameter model or spice model from IRIS EM simulation. Just by simple clicks, IRIS can replace devices or nets or the combination of both of them with iCell models. Then user can simulate the whole design with modified parts to check whether it meets the design specification by circuit simulation.



Back Annotation

to review the current distribution of device, which provides physical insights.



Current Density Display

Current Density Display

The display of current density enables users

US Office

Seattle

14205 SE 36th St, Bellevue, WA 98006

Silicon Valley

19925 Stevens Creek Blvd #100 Cupertino, CA 95014

sales@xpeedic.com

China, Shanghai Office

No.608, ShengXia Road, Building 2, Room210-211, Pudong New Area, Shanghai, 201203

Tel: 86 021 61636350

sales@xpeedic.com

China, Suzhou Office

No.2358, Changan Road, Bldg 1, Floor 5, Wujiang, Suzhou, 215200

Tel: 86 512 63989910

sales@xpeedic.com